

Table of Contents

About This Manual

1. VHDL Simulation Environment Setup

Setup Files	1-2
Library Name Mapping	1-3
Setup Variables	1-4
ASSERT_IGNORE	1-4
ASSERT_STOP.....	1-5
BROWSER_EXEC.....	1-5
BROWSER_NUMLISTS	1-5
COMPONENT_BINDING.....	1-6
CS_ASSERT_STOP_NEXT_WAIT	1-6
CS_CC PATH_ARCH	1-7
CS_CCFLAGS_ARCH.....	1-7
CS_COMPILED_WARN	1-9
CS_DEBUG.....	1-9
CS_NOCHECK	1-10

CY_CCPATH	1-10
CY_CCFLAGS	1-11
CY_INFO	1-12
CY_LDFLAGS	1-12
CY_MAKEPATH	1-13
CY_MAKEFLAGS	1-13
CY_MODE	1-13
CYSIM_REWIND	1-14
CY_VALUE	1-14
DBX_ANALYZER_CMD	1-15
DEFAULT_ANALYZE_MODE	1-15
DUT	1-16
EDITCMD	1-17
GS_REPORT_BUS_CONTENTION	1-18
GS_REPORT_BUS_FIGHT	1-18
GS_REPORT_BUS_FLOAT	1-19
GVAN_EDITSTR	1-19
GVAN_STOP_ON_WARNS	1-19
HELPDIR	1-20
IEEE	1-20
MAX_HIERARCHY_DEPTH	1-20
NO_CONSTRAINT_MESG	1-21
NO_CONSTRAINT_XGEN	1-21
NO_HAZARD_MESG	1-21
NO_HAZARD_XGEN	1-21
OPEN_WFILE_APPEND_MODE	1-22

PROMPT_STD_INPUT	1-22
RESFUNC_OPT	1-22
RUNREAD	1-23
SAVE_WVMSGS	1-23
SDFNAMINGFILE	1-23
SDFWILDCARD	1-23
SETUPEXIT	1-24
SIMFILE_ENCRYPTION	1-24
SPC	1-24
SYNOPSYS	1-25
TIMEBASE	1-25
USE	1-25
USER_MENU	1-26
WAVEFORM	1-26
WAVES_EXEC	1-26
WIF2TAB_HDRLEN	1-27
WINDOW	1-27
Setup Display	1-28
 2. Simulation Commands and Options	
VHDL Invocation Commands	2-2
coverage	2-2
cyclone	2-4
cylab	2-4
cysim	2-8
gvan	2-10

simcompiled	2-11
simdepends	2-12
vhdlan	2-14
C Compiler Information	2-19
vhldlbox	2-20
vhdlsim	2-21
waves	2-27
Predefined Simulator Variables	2-28
VSS Input Control Variables	2-29
VSS Output Control Variables	2-30
VSS Monitor and Trace Control Variables	2-31
VSS Simulation Control Variables	2-32
VSS Simulation Status Variables	2-32
VHDL Hierarchy and Source Code Control Variables	2-34
Cyclone Status Variables	2-36
VSS Top-Level Generics	2-36
Changing the Generic Parameter Default Value	2-37
Assigning Generic Values from a Command File	2-37
Assigning a Generic Value from the Keyboard	2-38
WIF Stimulus Files	2-40
3. VSS Command Line Interface	
VSS Simulation Control Language Selectors	3-2
VSS Simulation Control Language Commands	3-4
/	3-4

?	3-5
!	3-6
\$	3-7
abort	3-7
abstime	3-7
assign	3-8
call	3-9
cd	3-9
close	3-10
comm	3-11
continue	3-12
Control-c	3-12
coverage	3-13
delete	3-15
disable	3-15
drivers	3-16
dump_memory	3-17
dut_quiet	3-19
echo	3-19
edit	3-20
enable	3-21
environment	3-22
end	3-22
evaluate	3-23
exit	3-23
flush	3-24

foreach	3-24
fprint	3-25
help	3-28
hold	3-29
icon	3-29
if	3-30
include	3-30
Reading a Command File	3-30
Reading an SDF File	3-31
list	3-32
lmsi	3-33
load_memory	3-34
local	3-35
logtime	3-36
lpbreak	3-36
lpcontinue	3-37
ls	3-37
monitor	3-38
netlist_dump	3-42
next	3-44
open	3-44
pwd	3-46
quit	3-46
redirect	3-46
rename	3-47
restart	3-47

run	3-48
set	3-50
shift	3-51
show.	3-52
slist.	3-53
status	3-54
step	3-54
stop	3-55
trace.	3-55
unicon	3-57
unset	3-57
vcdaddobjects	3-58
vcdaddports	3-60
vcdcomment.	3-61
vcddumpall.	3-61
vcddumpobjects.	3-61
vcdfile.	3-62
vcdflush	3-62
vcdlimit.	3-63
vcoff	3-63
vcdon	3-63
wfield	3-64
where	3-65
while.	3-66
wifin	3-67
wmove	3-67

wsize 3-67

4. Cyclone Command Line Interface

Cyclone Simulation Control Language Commands.....	4-2
assign.....	4-3
cd.....	4-3
checkpoint.....	4-3
Control-c.....	4-4
cy_info varray.....	4-4
cyclone_commands.....	4-5
cycontinue.....	4-5
cyrename.....	4-5
cylist.....	4-6
cytrace.....	4-7
cytrace Limitations.....	4-9
cytrace Data Format.....	4-9
delete.....	4-9
disable.....	4-10
dump_memory.....	4-10
edit.....	4-11
enable.....	4-12
forward.....	4-13
history.....	4-13
hold.....	4-15
include.....	4-15
info.....	4-15

jump	4-17
load_memory	4-17
ls	4-18
maxtime	4-19
monitor	4-19
now	4-24
pwd	4-24
quit	4-24
release	4-24
restore	4-24
rewind	4-25
run	4-26
set	4-26
stop	4-27
vcdaddobjects and vcddumpobjects	4-27
vcdaddobjects	4-27
vcdfile	4-28
Wildcards	4-28
 Cyclone Simulation Control Variables	4-29
base	4-29
bus_resolution_msgs	4-30
state_freq	4-30
 5. Synopsys Standard Packages	
Referencing Synopsys Packages	5-2
Synopsys Package Descriptions	5-3

Standard Logic Package (std_logic_1164)	5-6
std_logic Type.	5-6
Logical Functions	5-7
Signal Resolution Functions.	5-8
Type Conversion Functions	5-9
Standard Logic Miscellaneous Package (std_logic_misc)	5-10
Strength Type	5-10
Strength Parameters for Different Technologies.	5-11
Truth Tables	5-11
Strength Conversion Functions	5-11
Type Conversion Functions	5-12
Boolean Reduction Functions	5-14
Tri-State Buffers	5-15
Miscellaneous Functions	5-16
Components Package (std_logic_components).	5-16
Arithmetic Package (std_logic_arith)	5-16
unsigned and signed Types	5-17
Type Conversion Functions	5-20
Arithmetic Functions.	5-24
Comparison Functions	5-27
Shift Functions	5-28
Standard Logic Signed and Unsigned Packages (std_logic_signed, std_logic_unsigned)	5-30
Examples of Using the Packages.	5-31
Text I/O Package (std_logic_textio)	5-36
Resolution Types Package (tri_resolved)	5-37
Sparse Memory Package (mem_api)	5-37
Real Math Package (math_real)	5-39
Domain of Real Numbers	5-39

Real Number Constants	5-39
Real Number Functions	5-40
** (exponentiation)	5-40
ACOS (arc cosine)	5-41
ACOSH (arc hyperbolic cosine)	5-41
ASIN (arc sine)	5-41
ASINH (arc hyperbolic sine)	5-42
ATAN (arc tangent)	5-42
ATAN2 (arc tangent 2)	5-42
ATANH (arc hyperbolic tangent)	5-43
CBRT (cube root)	5-43
CEIL (ceiling)	5-43
COS (cosine)	5-44
COSH (hyperbolic cosine)	5-44
EXP (e exponentiation)	5-44
FLOOR	5-45
FMAX (floating point maximum)	5-45
FMIN (floating point minimum)	5-45
GET_RAND_MAX (get random maximum)	5-46
LOG (X) (natural logarithm)	5-46
LOG (BASE, X) (logarithm of arbitrary base)	5-47
RAND (random number generator)	5-47
ROUND	5-48
SIGN	5-48
SIN (sine)	5-48
SINH (hyperbolic sine)	5-49
SQRT (square root)	5-49
SRAND (seed of random number)	5-49
TAN (tangent)	5-50

TANH (hyperbolic tangent)	5-50
Use of RAND Function.	5-50
Pipeline Process Example	5-51
Cautions When Using RAND	5-52
Types of Exceptions	5-54
Error Message Format	5-55
Limitations	5-55
Attributes Package (attributes)	5-56
Restricting or Enhancing Access to Models	5-56
Attributes and Types for Non-VHDL Models	5-62
Mapping User-Defined Types to and from std_logic.	5-64
Cyclone Package (cyclone)	5-66
Statistical Distributions Package (distributions)	5-66
Random Distribution	5-68
Uniform Distribution	5-69
Gaussian Distribution	5-70
Poisson Distribution	5-71
Exponential Distribution	5-72
Queueing Packages (vhdlzq and vhdlq)	5-73
Priority Parameters, Wait Statements	5-73
Queue Instrumentation.	5-74
Examples of Queue Implementation	5-74
GTECH Library	5-75

Appendix A. VHDL Interface for Tables Optimization

VHDL Interface for Tables	A-2
Format Requirements	A-3

Semantics of Table Evaluation	A-4
Example	A-5
Command-Line Options for cylab	A-7
Error Messages	A-7
TblAttrMismatch Error	A-8
TblAttrVal Error	A-8
TblFnArgs Error	A-9
TblTblArg Error	A-10
TblVecArg Error	A-10
TblVecArgSz Error	A-11

Appendix B. Design Model Examples

vector_in	B-2
scalar_in	B-4
AND_OR Primitive	B-6
RAM	B-8
Synchronous Adder	B-11
Referencing Attributes	B-12
Special Delays for Three-State Gates	B-15
Queuing Packages	B-18

Appendix C. VHDL93 Features

IEEE Unsupported Standards	C-2
VSS Unsupported Features	C-2

VSS Supported Features C-3

Index