

Table of Contents

About This Manual

1. General Guidelines

VHDL Coding Style 1-2

VHDL Value and Character Limits. 1-7

2. Testbench Guidelines

General Testbench Guidelines 2-3

Clock Generation from the Testbench 2-5

Clock Generation from the Main Clock 2-8

Reset Generation 2-9

Data Generation 2-10

Stimulus and Response Files 2-16

Message Files 2-21

3. Design Guidelines

Pullups and Pulldowns	3-2
Vectorization and Loops	3-3
Combinatorial Logic.	3-5
Sequential Logic	3-7
Clock Generation.	3-8

4. Memory Model Guidelines

General Memory Guidelines	4-3
Sparse Memory Models	4-6
Dual Port Memories.	4-8

Appendix A. Templates for Register Inference

D Latches	A-2
D Latch.	A-2
D Latch with Asynchronous Reset or Set	A-5
D Latch with Asynchronous Reset and Set	A-6
D Flip-Flops	A-7
D Flip-Flop with Positive or Negative Edge Trigger	A-7
D Flip-Flop with Asynchronous Reset or Set	A-8
D Flip-Flop with Asynchronous Set and Reset	A-9
D Flip-Flop with Synchronous Reset or Set.	A-10
D Flip-Flop with Synchronous and Asynchronous Load	A-11

D Flip-Flop with Asynchronous Reset, Set, Load, and Synchronous Load	A-12
JK Flip-Flops	A-13
JK Flip-Flop	A-13
JK Flip-Flop with Asynchronous Reset and Set.	A-14
Toggle Flip-Flops	A-15
Toggle Flip-Flop with Asynchronous Reset or Set	A-15
Toggle Flip-Flops with Enable and Asynchronous Reset.	A-17

Appendix B. Supported Language Constructs for Scirocco Cycle and Cyclone

Cycle Simulation Policy	B-2
Design Units.	B-3
Data Types.	B-5
Declarations.	B-7
Specifications.	B-8
Names	B-9
Attributes	B-9
Operators.	B-11
Operands and Expressions	B-12
Subprograms	B-14
Sequential Statements.	B-14
Concurrent Statements	B-16
Predefined Language Environment	B-17
Cycle Testbench Policy	B-18
The textio Package	B-18

Wait Statements.	B-18
Multiple Clocks.	B-20
VHDL Reserved Words	B-21

Appendix C. Cycle Simulation and LRM Differences

Index